Remarks

Reconsideration of the rejection of the subject matter of claims 1-17 is requested. Claim 12 has been cancelled by this amendment. Consequently, claims 1-11 and 13-17 remain in the case.

Claims 1-9 and 12-17 stand rejected under 35 USC 103(a) as being unpatentable on the basis of U.S. Patent No. 6,060,380 issued to Subramanian et al in view of EP 0 394 722 in the name of Kudoh et al. Claims 10-11 stand rejected as being unpatentable on the basis of U.S. Patent No. 6,060,380 issued to Subramanian et al in view of EP 0 394 722 in the name of Kudoh et al in further view of U.S. Patent No. 6,162,587 issued to Yang et al.

Subramanian et al is directed to forming trench lines (116) and via holes (110) in a dual damascene process using silicon oxynitride as a hard mask (402). A first photoresist (404) is patterned to ultimately define the trench line (116) in a top insulating layer (118), and a second photoresist (406) is patterned to ultimately define the via hole (110) in a bottom insulating layer (112). Hardmasks (302, 304, and 402) are also used to define the features. Kudoh et al shows a method (Figs 5A – 5E) for connecting conductors (30 and 40) on different levels of an integrated circuit by means of pillars (42). A first photoresist layer (26) is formed over a gold layer (24) and grooves (28) are defined in the photoresist down to the gold layer so that the bottom conductors (30) can be formed by electroplating. A second photoresist layer (32) is then formed over the structure, and openings (34) are defined therein to expose the lower conductors. Pillars (36) are formed by electroplating within the openings (34). Subsequent to the removal of the photoresist layers, the upper level conductors (40) are formed in contact with the pillars (36).

Examiner contends that Subramanian et al discloses the features of the claimed invention except for providing a second elongated opening which is transverse and perpendicular to the trench. Examiner further contends, however, that Kudoh et al shows these features, and that it would be obvious to combine the teachings of Subramanian et al and Kudoh et al.

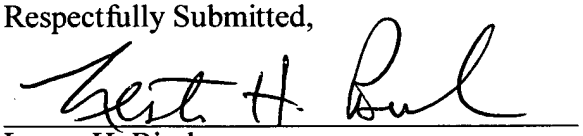
Claims 1, 13 and 14 have been amended to clearly distinguish over the cited art. In particular, those claims now include the limitation that no etch stop layer is used at the bottom of the trench. This feature finds support in the specification at page 5, lines 25-27,

and was formally included in claim 12 and now cancelled. Thus, a high dielectric interlayer, such as SiN, is avoided using the claimed process. Note that Subramanian et al employs a hard mask layer (302) as an etch stop before etching down to the conductor (102). (See Fig 4F.) Kudoh's groove (28) is etched to the conductor layer (24) to expose the metal for electroplating. Thus, neither reference discloses partially etching the dielectric to form a trench with a bottom in the dielectric without using an etch stop layer as now claimed.

It is submitted in view of the above that claims 1, 13, and 14 should be allowable. Since these claims are allowable, claims 2-11 and 15-17, which are dependent on claim 1, should also be allowable without the need for further discussion.

Passage to issue is requested.

Respectfully Submitted,



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Dated: 4/4/06